

REMARKS/ARGUMENTS

Claims 1-10 have been cancelled and new claims 21-38 are presented. It is respectfully submitted that new claim 21 overcomes the §112, ¶1 rejection and §112, ¶2 rejections of claim 1.

New claim 21 is patentable over the cited art, including U.S. Patent No. 6,647,502 (Ohmori), at least because Ohmori nowhere teaches a buffer coupled to an output of a first processor unit, where the buffer is clocked by a master clock and the processor unit is clocked by another clock generated by a clock controller. For at least this reason, claim 21 and claims 22-29 depending therefrom are patentable over Ohmori.

New claim 30 is patentable over the cited art, as neither Ohmori nor the other cited art teaches or suggests a controller to control a processor unit to optimize processing power based on a feedback signal from a buffer coupled to an output of the processor unit. Instead, Ohmori teaches that modules are controlled using signals obtained from an input side of the module, not an output side of the module. Accordingly, claims 30-35 are patentable over the cited art.

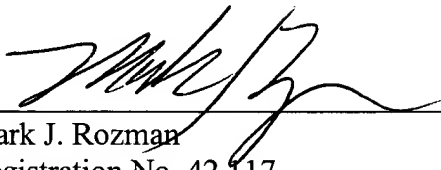
New claim 36 is patentable for at least the same reason discussed above regarding claim 21. That is, Ohmori and the other cited art nowhere teach or suggest clocking multiple processors with multiple clocks and clocking a buffer coupled between the processors with a master clock. Accordingly, for at least this reason, claim 36 and claims 37-39 are patentable over the cited art.

Enclosed herewith is a terminal disclaimer and accompanying fee to overcome the provisional obviousness-type double patenting objection over U.S. Patent Application No. 09/837,651.

The application is believed to be in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

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Respectfully submitted,



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